CLAIMS

I claim:

1. A crossbar switch circuit, comprising:

a plurality of ports coupled to a bus;

at least one memory element coupled to one of said plurality of ports; and

a circuit for generating a write enable pulse coupled to each of said at least one memory element, comprising:

a pulse generator for generating a pulse, said pulse tracking a leading edge of a clock signal;

a write enable signal generator for generating a write enable signal; and

a first logic circuit coupled to said pulse generator and said write enable signal generator for generating said write enable pulse by combining said pulse and said write enable signal.

2. The crossbar switch circuit of claim 1, wherein said pulse generator comprises:

a device for generating an output signal in response to said clock signal;

a first delay circuit for generating a first delay signal in response to said output signal;

a second delay circuit coupled to said first delay circuit, said second delay circuit generating a second delay signal in response to said first delay signal; and

a second logic circuit coupled to said first delay circuit and said second delay circuit, said second logic circuit generating said pulse by combining said first delay signal and said second delay signal.

3. The crossbar switch circuit of claim 2, wherein said device comprises a toggle flip-flop.

4. The crossbar switch circuit of claim 2, wherein said first delay circuit includes at least one delay element.

5. The crossbar switch circuit of claim 4, wherein said first delay circuit includes a plurality of delay elements, said delay elements being selected from the group consisting of inverting delay elements and noninverting delay elements.

6. The crossbar switch circuit of claim 2, wherein said second delay circuit includes at least one delay element.

7. The crossbar switch circuit of claim 6, wherein said second delay circuit includes a plurality of delay elements, said delay elements being selected from the group consisting of inverting delay elements and noninverting elements.

8. The crossbar switch circuit of claim 1, wherein said write enable signal generator comprises a register for registering an external write enable signal, said register being clocked by said clock signal.

9. The crossbar switch circuit of claim 1, wherein said write enable signal generator comprises a plurality of registers for registering a plurality of external write enable signals, further comprising a selector for selecting a registered external write enable signal.

10. The crossbar switch circuit of claim 1, further comprising a data bus for coupling each of said plurality of ports to a data input of said at least one memory element.

11. The crossbar switch circuit of claim 1, wherein said at least one memory element comprises a RAM (random access memory).

12. The crossbar switch circuit of claim 11, wherein said RAM comprises an asynchronous RAM.

13. The crossbar switch circuit of claim 1, wherein a first port of said plurality of ports comprises a plurality of memory elements, further comprising a first selector coupled to

said plurality of memory elements, said first selector being coupled to said bus.

14. The crossbar switch circuit of claim 1, wherein a first port of said plurality of ports comprises a plurality of memory elements, further comprising:

a first selector coupled to said plurality of memory elements;

a second selector coupled to a second port of said plurality of ports; and

a third selector coupled to said first selector and said second selector, said third selector being coupled to said bus.

15. A computer system, comprising:

a crossbar switch comprising:

a plurality of ports coupled to a bus;

at least one memory element coupled to one of said plurality of ports; and

a circuit for generating a write enable pulse coupled to each of said at least one memory element, comprising:

a pulse generator for generating a pulse, said pulse tracking a leading edge of a clock signal;

a write enable signal generator for generating a write enable signal; and

a first logic circuit coupled to said pulse generator and said write enable signal generator for generating said write enable pulse by combining said pulse and said write enable signal; and

at least one processing unit coupled to each of said plurality of port.

16. The computer system of claim 15, wherein said at least one processing unit comprises a processing unit selected from the group consisting of CPUs (central processing units) and I/O (input/output) processors.

17. The computer system of claim 15, wherein a plurality of processing units are

coupled to a first port, further comprising a selector for selecting one processing unit from said plurality of processing units.

18. The computer system of claim 15, wherein said processing unit is an I/O (input/output) processor, further comprising an I/O buffer coupled between said port and said I/O processor.

19. The computer system of claim 15, wherein said pulse generator comprises:

a device for generating an output signal in response to said clock signal;

a first delay circuit for generating a first delay signal in response to said output signal;

a second delay circuit coupled to said first delay circuit, said second delay circuit generating a second delay signal in response to said first delay signal; and

a second logic circuit coupled to said first delay circuit and said second delay circuit, said second logic circuit generating said pulse by combining said first delay signal and said second delay signal.

20. The computer system of claim 19, wherein said first delay circuit includes at least one delay element.

21. The computer system of claim 20, wherein said first delay circuit includes a plurality of delay elements, said delay elements being selected from the group consisting of inverting delay elements and noninverting delay elements.

22. The computer system of claim 19, wherein said second delay circuit includes at least one delay element.

23. The computer system of claim 22, wherein said second delay circuit includes a plurality of delay elements, said delay elements being selected from the group consisting of inverting delay elements and noninverting elements.

24. The computer system of claim 15, wherein said write enable signal generator comprises a register for registering an external write enable signal, said register being clocked by said clock signal.

25. The computer system of claim 15, wherein said write enable signal generator comprises a plurality of registers for registering a plurality of external write enable signals, further comprising a selector for selecting a registered external write enable signal.

26. A method for communicating between a first processing unit coupled to a first port of a crossbar switch and a second processing unit coupled to a second port of said crossbar switch, comprising:

generating a request for a communication path from said first processor to said second processor;

transmitting data from said second processor to said first port;

storing said data in a memory element in said first port, comprising:

generating a pulse in response to a clock signal, said pulse tracking a leading edge of said clock signal;

generating a write enable signal; and

generating a write enable pulse by combining said pulse and said write enable signal; and

reading said data from said memory element.

27. The method of claim 26, wherein generating a pulse comprises:

generating an output signal in response to said clock signal;

delaying said output signal to generate a first delay signal;

delaying said first delay signal to generate a second delay signal; and

performing a first logic function on said first delay signal and said second delay signal, thereby generating said pulse.

28. The method of claim 27, further comprising arranging at least one delay

elements in accordance with a predetermined setup time and a predetermined hold time, said at least one delay elements being selected from the group consisting of inverting delay elements and noninverting delay elements.

29. The method of claim 27, further comprising determining said first logic function in accordance with a first polarity of said first delay signal and a second polarity of said second delay signal.

30. The method of claim 26, wherein generating a write enable signal comprises registering at least one external write enable signal.

31. The method of claim 30, wherein a plurality of external write enable signals are registered, further comprising:

selecting a registered external write enable signal; and

generating said write enable signal from a selected registered external write enable signal.

32. The method of claim 26, wherein combining said pulse and said write enable signal comprises:

performing a second logic function; and

determining said second logic function in accordance with whether said write enable pulse is active high or active low.